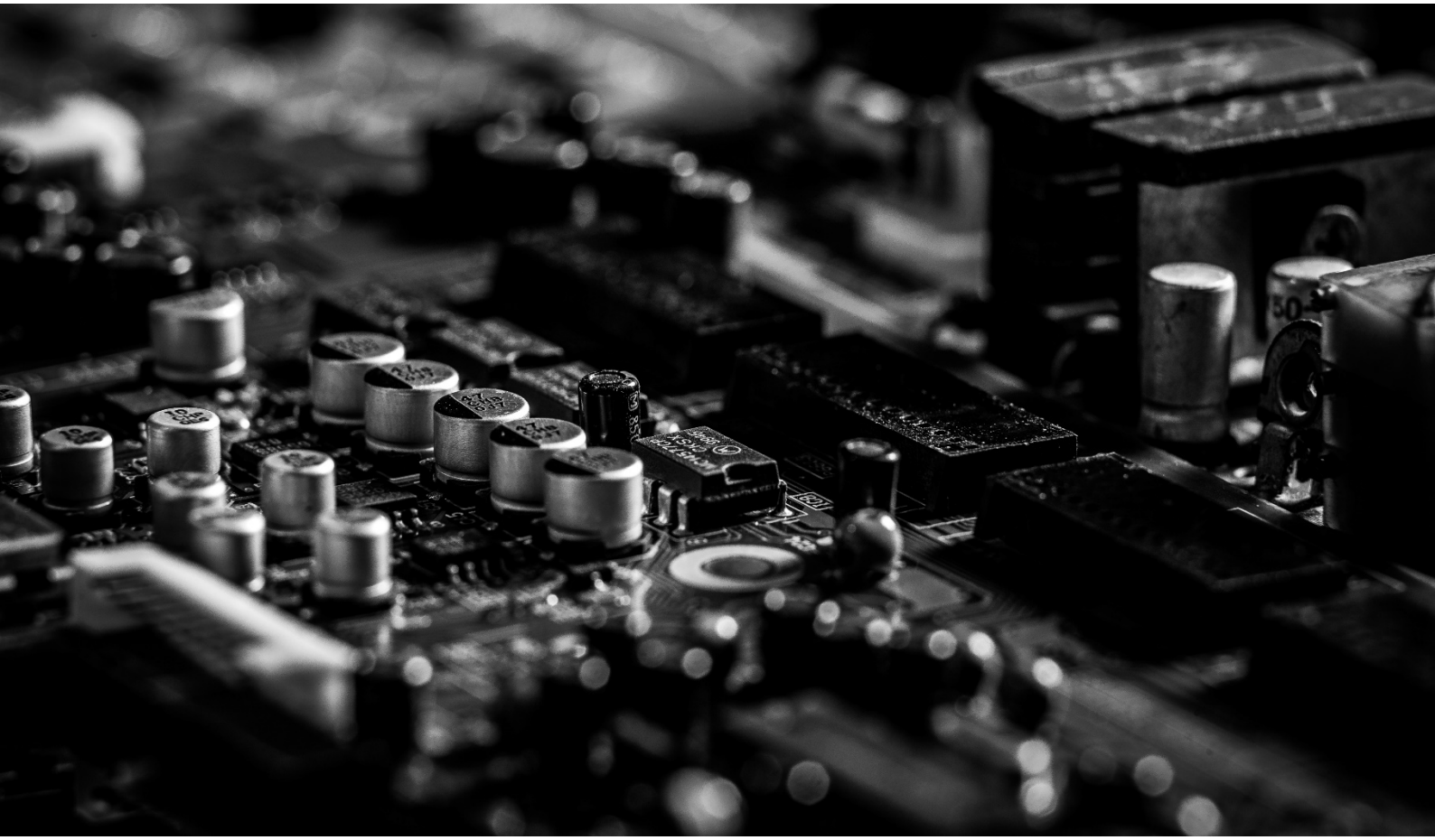
复锦功率半导体
FUJIN POWER SEMICONDUCTOR



FJ05S06NAL-A Draft Datasheet

FJ05S06NAL 3.0V to 5.7V Input, 6A Synchronous Buck, Integrated Power Solution

Date:2023-1

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CHENGDU FUJIN POWER SEMICONDUCTOR TECHNOLOGY DEVELOPMENT CO., LTD

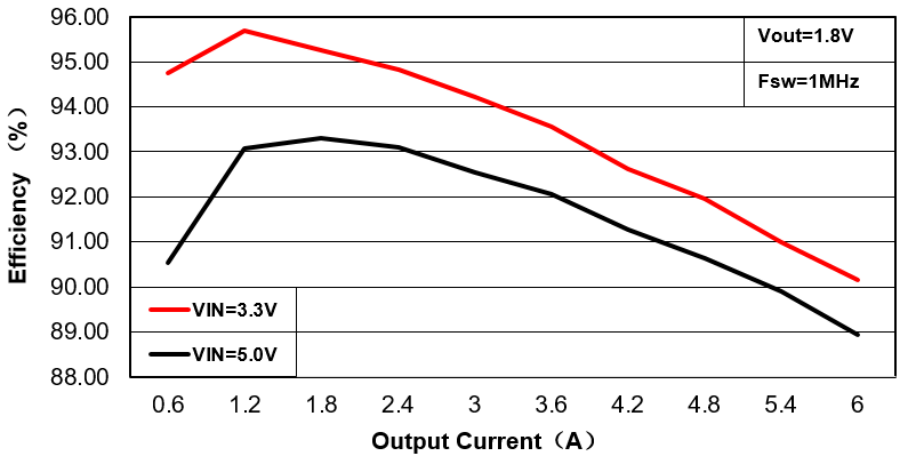
CONTENTS

1 Features

- Highly integrated power solution allows small footprint, low profile
- Peak maximum efficiency up to 97%
- 0.9V to 3.7V output voltage adjustable with 1% accuracy
- Pre-bias output start-up
- Programmable undervoltage lockout (UVLO)
- Cycle-by-cycle current limit and hiccup current protection (OCP)
- Over temperature protection (OTP)
- Output overvoltage protection (OVP)
- Output short protection (OSP)
- Power good output
- Operating temperature range: -40℃ to +85℃

2 Applications

- Servers and telecom
- Automated test and industrial equipment
- Point of load regulation for high-performance
- Low-voltage, high-density power systems



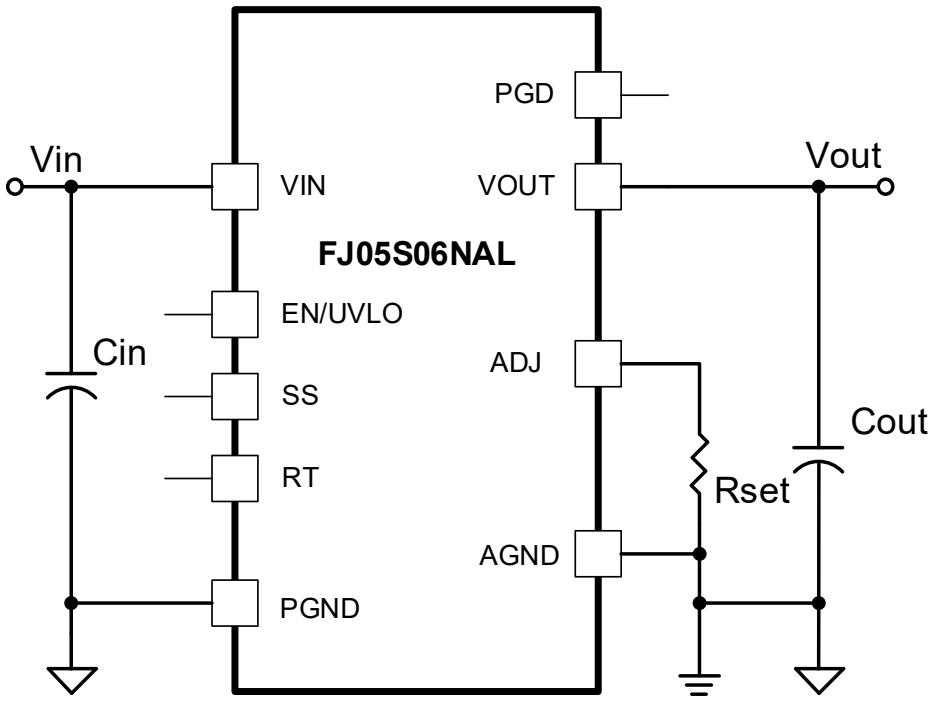
3 Description

The FJ05S06NAL is an easy-to-use power system integrated in package solution that combines an 6A converter, a power inductor and passives into a low profile, QFN package. This modularity power solution allows as few as 3 external components and eliminates complicated loop compensation design and magnetic device selection.

The 7x7x4mm QFN package is easy to solder onto PCB and allows a compact POL design with greater than 90% efficiency. The device delivers 6A rated output current at +85℃ ambient temperature without airflow.

The FJ05S06NAL offers the flexibility point of load design and is ideal for powering performance digital devices. The advanced packaging techology afford a robust and reliable power solution.

Simplified Application



4 Specifications

4.1 Absolute Maximum Ratings (1)

		MIN	MAX	Unit
Input Voltage	VIN, EN/UVLO	-0.3	7	V
	PGD	-0.3	6	V
	COMP, SS, RT, ADJ	-0.3	3	V
Output Voltage	BOOT		7	V
	SW	-0.3	7	
	SW (20 ns transient)	-2	10	V
	SW (5 ns transient)	-4	12	V
Source current	EN/UVLO, RT		100	μA
Sink current	COMP, SS		100	μA
	PGD		10	mA
Operating junction temperature			-40 to 125(2)	℃
Storage junction temperature			-65 to 150	℃
Peak reflow case temperature			260	℃
Maximum number of reflows allowed			3	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stresses rating only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

(2) See the temperature derating curves in the typical characteristics section for the thermal information

4.2 Thermal Information

Thermal Metric		FJ05S06NAL	UNITS
		39 PINS	
θ_{JA}	junction to ambient thermal resistance	44	℃/W
θ_{JCtop}	junction to case (top) thermal resistance	46	
θ_{JB}	junction to board thermal resistance	16	

4.3 Package Specifications

FJ05S06NAL		UNIT
Weight		g
Size	7x7x4 (LxWxH)	mm
Flammability	Meet UL94 V-O (refer to TI)	
MTBF calculated	Per Bellcore TR-332, 50% stress, Ta=40℃, ground	33 MHrs

reliability	denign	

4.4 Electrical characteristics

Over -40℃ to +85℃ free air temperature, V_{IN}=5.0V, V_{OUT}=1.8V, I_{max}=6A, C_{IN1}=100μF AL- electrolytic capacitor, C_{IN2}=47μF ceramic, C_{OUT1}=1x100μF ceramic (unless otherwise noted)

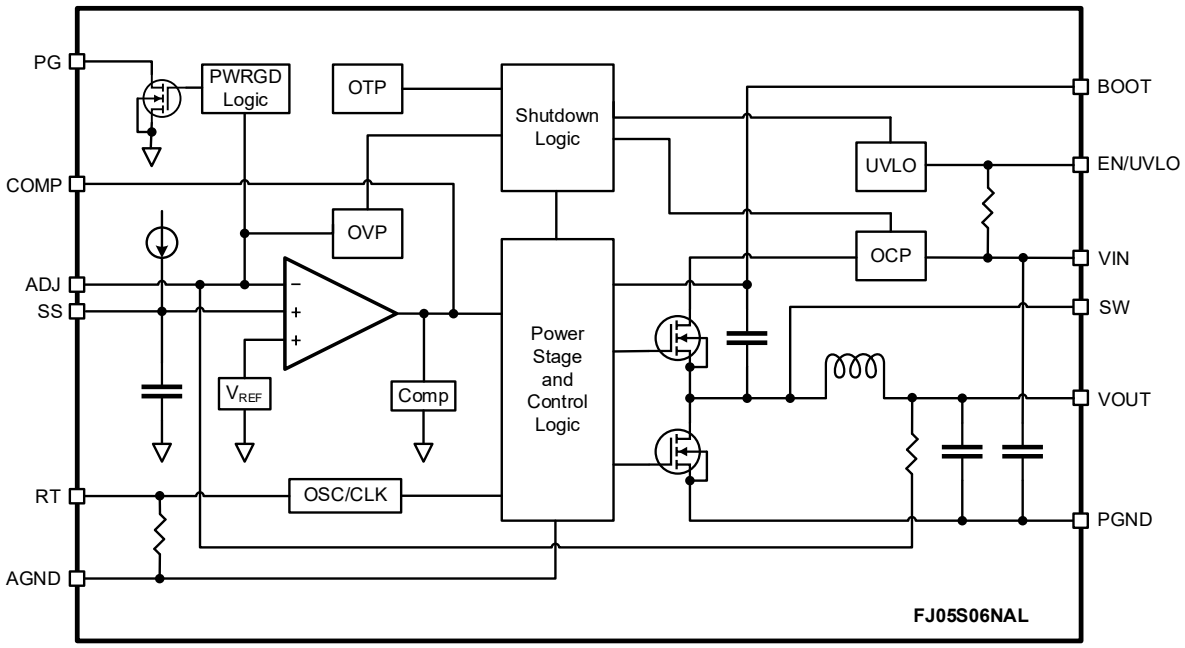
Parameter		Test condition	MIN	TYP	MAX	UNIT
I_{OUT}	Output current	TA 85℃, natural convection	0		6	A
V_{IN}	Input bias voltage range	Over Iout range	3.0		5.7	V
UVLO	VIN undervoltage lockout	VIN increasing threshold	2.6	2.76	2.87	V
		VIN decreasing threshold	2.33	2.48	2.6	V
$V_{OUT(adj)}$	Output voltage adjust range,	Over Iout range; Vin - Vout > 0.5V	0.9		3.7	V
V_{OUT}	Set point voltage tolerance,	-40℃~+85℃;VIN=3.3V/5.0V; Iout=50% of Imax; with 1% tolerance external resistor to set output voltage.			±1%	
	Temperature variation	-40℃~+85℃, Iout=50% of Imax			±1%	
	Line regulation	Over VIN range, Ta=25℃, Iout=50% of Imax			±0.1 %	
	Load regulation	Over load range, Ta=25℃			±0.1 %	
	Total output voltage variation	-40℃~+85℃; Over VIN range, over load range			±2%	
η	Efficiency 50% load	Vin=3.3V, Vout=0.9V, T_A=25℃		89.3		%
		Vin=3.3V, Vout=1.0V, T_A=25℃		89.9		%
		Vin=3.3V, Vout=1.2V, T_A=25℃		91.7		%
		Vin=3.3V, Vout=1.5V, T_A=25℃		93.1		%
		Vin=3.3V, Vout=1.8V, T_A=25℃		94.2		%
		Vin=3.3V, Vout=2.5V, T_A=25℃		95.8		%
		Vin=5.0V, Vout=0.9V, T_A=25℃		87.8		%
		Vin=5.0V, Vout=1.0V, T_A=25℃		88.6		%
		Vin=5.0V, Vout=1.2V, T_A=25℃		90.0		%
		Vin=5.0V, Vout=1.5V, T_A=25℃		91.6		%
		Vin=5.0V, Vout=1.8V, T_A=25℃		92.5		%
		Vin=5.0V, Vout=2.5V, T_A=25℃		94.5		%
		Vin=5.0V, Vout=3.3V, T_A=25℃		95.9		%
		Vin=5.0V, Vout=3.7V, T_A=25℃		96.3		%
	Efficiency 100% load	Vin=3.3V, Vout=0.9V, T_A=25℃		82.3		%
		Vin=3.3V, Vout=1.0V, T_A=25℃		83.7		%
		Vin=3.3V, Vout=1.2V, T_A=25℃		86.4		%
		Vin=3.3V, Vout=1.5V, T_A=25℃		88.3		%
		Vin=3.3V, Vout=1.8V, T_A=25℃		90.1		%
		Vin=3.3V, Vout=2.5V, T_A=25℃		92.8		%
		Vin=5.0V, Vout=0.9V, T_A=25℃		81.1		%
		Vin=5.0V, Vout=1.0V, T_A=25℃		82.4		%
		Vin=5.0V, Vout=1.2V, T_A=25℃		84.6		%
		Vin=5.0V, Vout=1.5V, T_A=25℃		87.1		%
		Vin=5.0V, Vout=1.8V, T_A=25℃		88.9		%
		Vin=5.0V, Vout=2.5V, T_A=25℃		91.7		%
		Vin=5.0V, Vout=3.3V, T_A=25℃		93.5		%

		Vin=5.0V, Vout=3.7V, T_A=25℃		94.1		%
$Vout_{ripple}$	Output voltage ripple	20 MHz bandwith; over Iout range; over Vin range; over Vout range		10	18	mV
$Vout_{noise}$	Output voltage noise	500 MHz bandwith; over Iout range; over Vin range; over Vout range		20	50	mV
I_{LIMT}	Output overcurrent protection	Hiccup mode	6.5	8	12	A
Transient response recovery time		load step from 25% to 50% Imax; 1.0A/us				
		load step from 50% to 75% Imax; 1.0A/us				
Transient response overshoot amplitude		load step from 25% to 50% Imax; 1.0A/us				
		load step from 50% to 75% Imax; 1.0A/us				
Power good	PGD threshold	ADJ rising GOOD		93		%Vref
		ADJ falling Fault		91		%Vref
		ADJ rising Fault		116		%Vref
		ADJ falling GOOD		114		%Vref
		Power good output low (Ipgd=2.5mA)			0.3	V
fsw	Switching frequency	Over VIN and Iout range; RT pin open		1		MHz
C_{IN}	External input capacitance	Ceramic	47			μF
		Non- ceramic	68			μF
C_{OUT}	External output capacitance	Ceramic	100		1600	μF
		Non- ceramic		220	2000	μF
		Equivalent series resistance (ESR)			50	mΩ
Thermal shutdown		Thermal shutdown				
		Thermal shutdown hysteresis				

the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. the overrall output voltage tolerance will be affected by the tolerance of the external Rset resistor.

5 Device Information

5.1 Functional Block Diagram

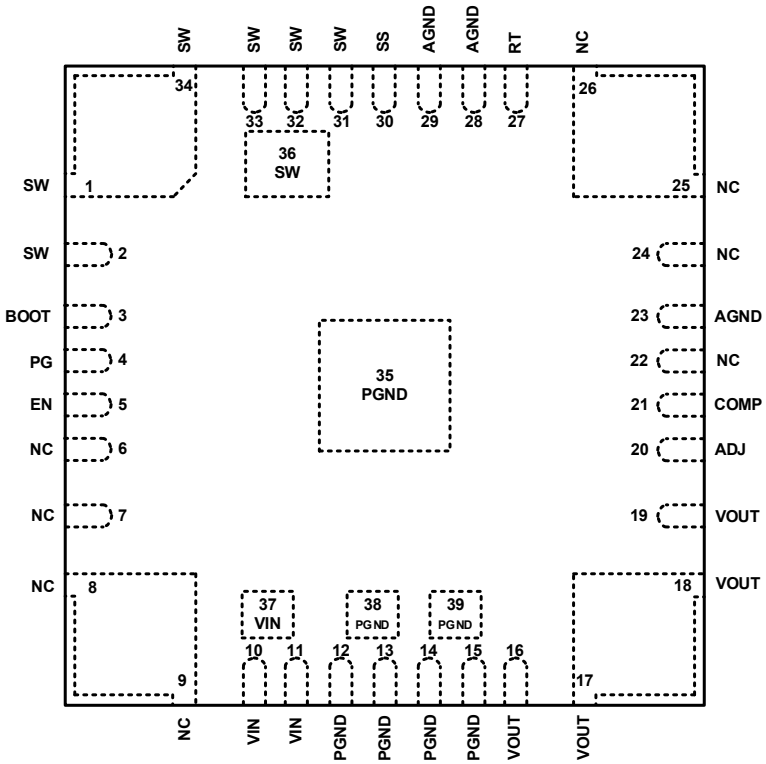


5.2 PIN Descriptions

Terminal		Description
Name	NO.	
SW	1	Switching node. the source of the internal high-side power MOSFET, drain of the internal low-side rectifier MOSFET, and one end of internal power inductor. These pins should be connected by a small copper island under the device for thermal relief. Do not place any external component on these pins or tie it to a pin of another function.
	2	
	31	
	32	
	33	
	34	
	36	
BOOT	3	Bootstrap. Internal there is a bootstrap capacitor connected between BOOT and SW. do not connect this pin to any external component or tie it to any other function.

PG	4	Power good fault pin. An open-drain output asserts low if output voltage is low due to thermal shutdown, overvoltage, undervoltage, or EN shutdown. An external pull-up resistor is required.
EN/UVLO	5	Enable or UVLO pin. Internal 10kΩ pull-up resistor to VIN. Float to enable. Can be used to set the on and off threshold (adjust UVLO) with additional resistor.
NC	6	Not connect. These pins must remain isolated from one another. Do not connect these pins to AGND or to any voltage. These pins must be soldered to isolated pads.
	7	
	8	
	9	
	22	
	24	
	25	
	26	
VIN	10	Input bias voltage pin. Supplies the control circuitry of the power converter.
	11	
	37	
PGND	12	Common ground connection for the VIN and VOUT power connections.
	13	
	14	
	15	
	35	
	38	
	39	
VOUT	16	Output voltage. Connect output capacitors between these pins and PGND.
	17	
	18	
	19	
ADJ	20	Connecting a resistor between this pin and AGND sets the output voltage.
COMP	21	Error amplifier output. Internal loop compensation RC network, do not place any external components on this pin.
AGND	23	Analog ground should be electrically connected to GND close to the device.
	28	
	29	
RT	27	Switching frequency setting pin.
SS	30	Soft start time setting pin.

5.3 Package top view



6 Typical characteristics (VIN=3.3V)

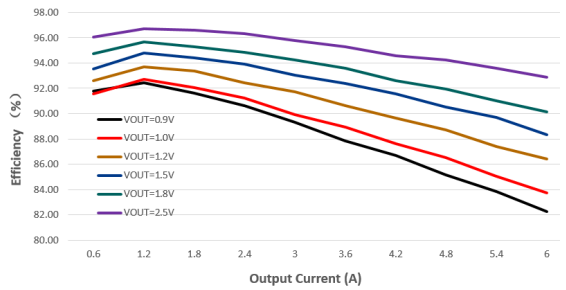


Figure 1. Efficiency vs. Output current

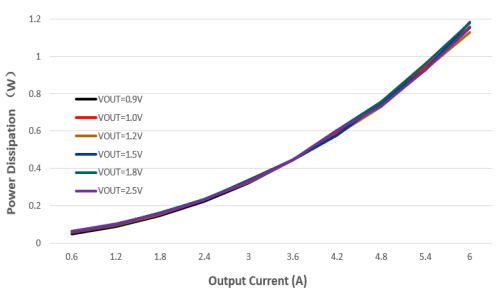


Figure 2. Power dissipation vs. Output current

Figure 3. Safe operating Area

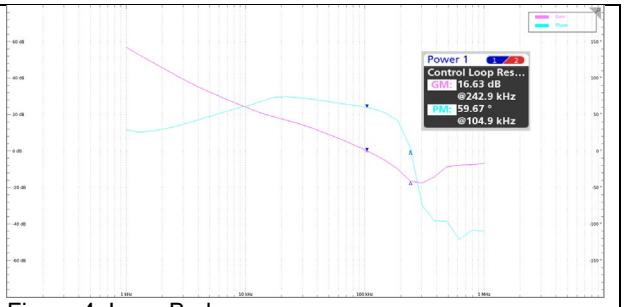


Figure 4. Loop Bode
VIN=3.3V, VOUT=1.0V, Iout=3A, Cout1=5x100μF MLCC, Cout2=0μF SPCAP

7 Typical characteristics (VIN=5.0V)

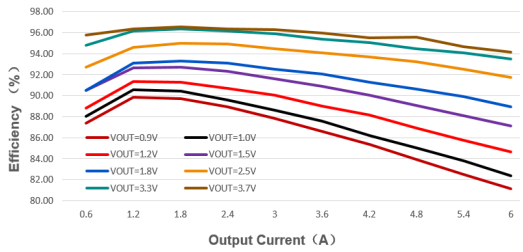


Figure 5. Efficiency vs. Output current

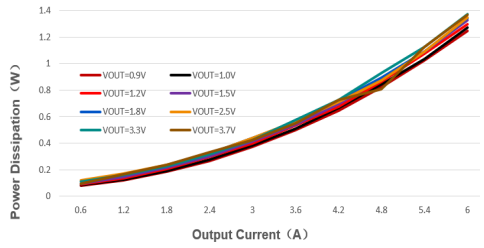


Figure 6. Power dissipation vs. Output current

Figure 7. Safe operating Area

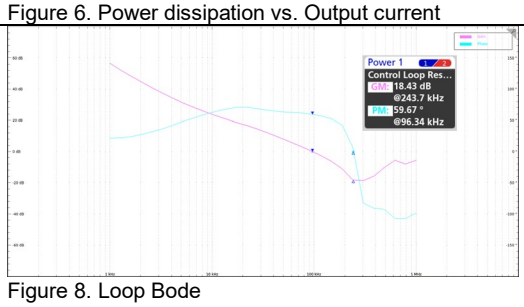


Figure 8. Loop Bode
VIN=5.0V, VOUT=1.0V, Iout=3A, Cout1=5x100μF MLCC, Cout2=0μF SPCAP

8 Application information

8.1 Adjust the output voltage

the ADJ control the output voltage of FJ05S06NAL. The output voltage adjustment range is from 0.9V to 3.7V. the adjustment method requires the additional Rset which sets the output voltage value, the Rset resistor must be connected directly between ADJ and AGND.

Table 3 gives the standard external Rset resistor for a number of common bus voltage,

Table 3. Standard Rset Resistor Value for Common Output Voltages

Resistor	Output Voltage Vout (V)					
	1.0	1.2	1.5	1.8	2.5	3.3
Rset (kΩ)	30	20	13.333	10	6.316	4.444

For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in table 4.

$$Rset = \frac{20}{\frac{Vout}{0.6} - 1}(k\Omega)$$

Table 4. Standard Rset Resistor Values

Vout (V)	Rset (kΩ)		Vout (V)	Rset (kΩ)
0.9	40		2.4	6.667
1.0	30		2.5	6.316
1.1	24		2.6	6
1.2	20		2.7	5.714
1.3	17.143		2.8	5.455
1.4	15		2.9	5.217
1.5	13.333		3.0	5
1.6	12		3.1	4.8
1.7	10.909		3.2	4.615
1.8	10		3.3	4.444
1.9	9.231		3.4	4.286
2.0	8.571		3.5	4.138
2.1	8		3.6	4
2.2	7.5		3.7	3.871
2.3	7.059			

8.2 Capacitor Recommendation for FJ05S06NAL power supply

8.2.1 Capacitor Selection

8.2.1.1 Electrolytic, Poly-Electrolytic Capacitors

When using electrolytic capacitors, high-quality, high temperature grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0℃. The lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size can be as polymer-electrolytic capacitors selection requirement. Aluminum electrolytic capacitors provide adequete decoupling over the frequency range of 2kHz TO 50kHz, and suitable when ambient temperatures are above 0℃.

8.2.1.2 Ceramic Capacitors

The performance of aluminum electrolytic capacitor is less effective than ceramic capacitor above 150kHz. Multi-layer ceramic capacitors have a low ESR and a high resonant frequency. They can be used to reduce reflected ripple current at the input as well as improve the transient response of the output. X5R and X7R ceramic dielectrics or equivalent for power application since they have high capacitance to volume ratio and are fairly stable over temperature. The capacitor selection need take the DC bias and AC voltage derating into consideration. The derated capacitance value of a ceramic capacitor due to DC voltage bias and AC RMS voltage is usually found on the capacitor manufacture's website.

8.2.2 Input Capacitor Selection

Input decoupling ceramic capacitors type X5R, X7R from VIN to GND that are placed as close as possible to the FJ05S06NAL VIN pins. A total of at least 47μF capacitance is required and some applications can require a bulk capacitance. At least 47μF of bypass capacitance is recommended as close as possible to VIN pin to minimize the input voltage ripple. A 0.1μF to 1μF capacitor must be placed as close as possible to VIN to provide high frequency bypass to reduce the high frequency overshoot and undershoot. The voltage rating of the input capacitor must be greater than the maximum input voltage.

8.2.3 Output Capacitor Selection

The required output capacitance is determined by the output voltage of FJ05S06NAL. The required output capacitance can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 1x100μF ceramic capacitor. When adding additional non-ceramic bulk capacitors, low ESR devices. The required capacitance above the minimum is determined by actual transient deviation requirement.

Table 6. Output Voltage Transient Response

Cin1=1x47μF ceramic, Cin2=100μF SP-CAP, Load Step=3A,1A/μs					
Vout (V)	VIN (V)	Cout1 Ceramic	Cout2 Bulk	Peak to Peak (mV)	Recovery time (μs)
0.9	3.3	1x100μF	NC		
		1x47μF	330μF		
	4.5	1x100μF	NC		
		1x47μF	330μF		
	5.0	1x100μF	NC		

		1x47μF	330μF		
1.0	3.3	1x100μF	NC		
		1x47μF	330μF		
	4.5	1x100μF	NC		
		1x47μF	330μF		
	5.0	1x100μF	NC		
		1x47μF	330μF		
1.2	3.3	1x100μF	NC		
		1x47μF	330μF		
	4.5	1x100μF	NC		
		1x47μF	330μF		
	5.0	1x100μF	NC		
		1x47μF	330μF		
1.5	3.3	1x100μF	NC		
		1x47μF	330μF		
	4.5	1x100μF	NC		
		1x47μF	330μF		
	5.0	1x100μF	NC		
		1x47μF	330μF		
1.8	3.3	1x100μF	NC		
		1x47μF	330μF		
	4.5	1x100μF	NC		
		1x47μF	330μF		
	5.0	1x100μF	NC		
		1x47μF	330μF		
2.5	3.3	1x100μF	NC		
		1x47μF	330μF		
	4.5	1x100μF	NC		
		1x47μF	330μF		
	5.0	1x100μF	NC		
		1x47μF	330μF		
3.3	4.5	1x100μF	NC		
		1x47μF	330μF		
	5.0	1x100μF	NC		
		1x47μF	330μF		
	5.5	1x100μF	NC		
		1x47μF	330μF		
3.7	4.5	1x100μF	NC		
		1x47μF	330μF		
	5.0	1x100μF	NC		
		1x47μF	330μF		
	5.5	1x100μF	NC		
		1x47μF	330μF		

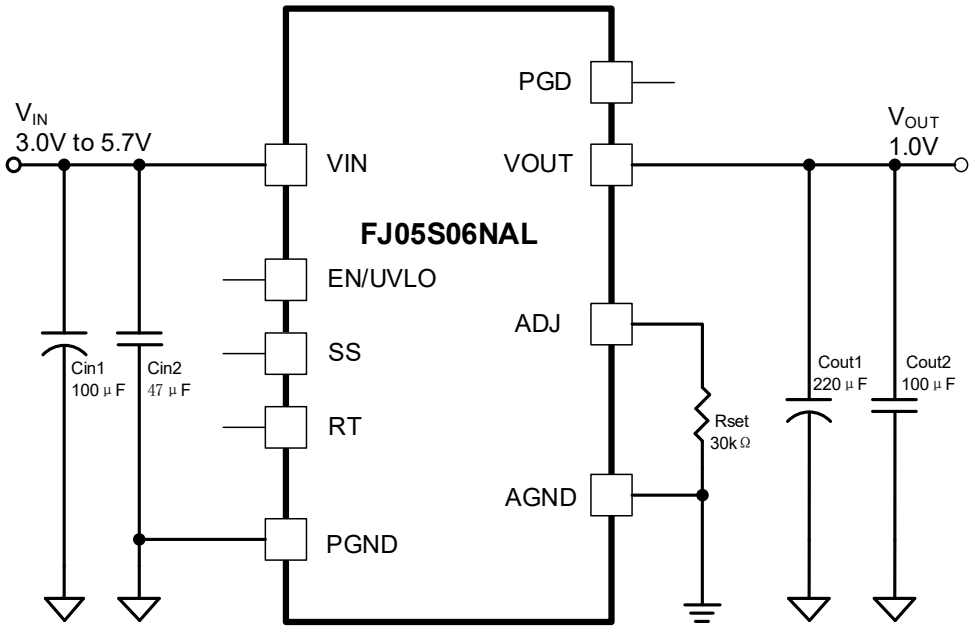
Table 7. Recommended Input / Output Capacitors

Vendor	Series	Part Number	Capacitor Characteristics		
			Working Voltage (V)	Capacitance (μF)	ESR (mΩ)

8.3 Transient Response

Figure 17. Vin=3.3V, Vout=0.9V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us	Figure 18. Vin=3.3V, Vout=1.0V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us
Figure 19. Vin=3.3V, Vout=1.2V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us	Figure 20. Vin=3.3V, Vout=1.5V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us
Figure 21. Vin=3.3V, Vout=1.8V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us	Figure 22. Vin=3.3V, Vout=2.5V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us
Figure 23. Vin=5.0V, Vout=0.9V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us	Figure 24. Vin=5.0V, Vout=1.0V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us
Figure 25. Vin=5.0V, Vout=1.2V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us	Figure 26. Vin=5.0V, Vout=1.5V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us
Figure 27. Vin=5.0V, Vout=1.8V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us	Figure 28. Vin=5.0V, Vout=2.5V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us
Figure 29. Vin=5.0V, Vout=3.3V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us	Figure 30. Vin=5.0V, Vout=3.7V, Cout1=47μF ceramic, Cout2=330μF SPCAP, 3A step, 1kHz, 1A/us

8.4 Application Schematic



8.5 VIN input voltage

The VIN voltage supplies the internal control circuits and power converter system of the device. The input voltage for the VIN pin can range from 3.0V to 5.7V. a voltage divider connected to

EN pin can adjust the either input voltage UVLO appropriately. See the Programmable Undervoltage Lockout (UVLO) section of this datasheet for more information.

8.6 Power Good (PGD)

The PWRGD pin is an open drain output. Once the voltage on the ADJ pin is between 94% and 106% of the set voltage, the PWRGD pin pull-down is released and the pin floats. The recommended pull-up resistor value is between 10kΩ and 100kΩ to a voltage source that is 5.5V or less. The PWRDG pin is pulled low when the voltage on ADJ is lower than 91% or greater than 109% of the nominal set voltage. Also, the PWRDG pin is pulled low if the input UVLO or thermal shutdown is asserted, the EN pin is pulled low, or the SS pin is below 1.4V.

8.7 Power-up characteristics

When configured as shown in front page schematic, the FJ05S06NAL produce a regulated output voltage following the application of a vaild input voltage. During the power-up, the internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of inrush current that can be drawn from the input source. The soft-start cricuitry introduces a short time delay from the point that a vaild input voltage is recongnized. Figure 28 shows the start-up waveforms for a FJ05S06NAL, operating from a 5V input and with the output adjusted to 1.8V. figure 29 shows the start-up waveforms for a FJ05S06NAL starting up into a pre-biased output voltage.

Figure 31. Vin=3.3V, Vout=1.0V, 6A load, start-up waveforms	Figure 32. Vin=3.3V, Vout=1.0V, start-up into pre-bias
Figure 33. Vin=3.3V, Vout=1.5V, 6A load, start-up waveforms	Figure 34. Vin=3.3V, Vout=1.5V, start-up into pre-bias
Figure 35. Vin=3.3V, Vout=2.5V, 6A load, start-up waveforms	Figure 36. Vin=3.3V, Vout=2.5V, start-up into pre-bias
Figure 37. Vin=5.0V, Vout=1.2V, 6A load, start-up waveforms	Figure 38. Vin=5.0V, Vout=1.2V, start-up into pre-bias
Figure 39. Vin=5.0V, Vout=1.8V, 6A load, start-up waveforms	Figure 40. Vin=5.0V, Vout=1.8V, start-up into pre-bias
Figure 41. Vin=5.0V, Vout=3.3V, 6A load, start-up waveforms	Figure 42. Vin=5.0V, Vout=3.3V, start-up into pre-bias

8.8 Pre-Biased Start-up

The FJ05S06NAL has been designed to prevent discharging a pre-biased output. During monotonic pre-biased startup, the FJ05S06NAL does not allow current to sink until the SS pin voltage is higher than 1.4V.

8.9 Output ON/OFF

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use an open drain/collector device. Or a suitable logic gate to interface with the pin.

Figure 30. shows the typical application of the EN/UVLO function. The EN control has its own internal pull-up to VIN potenial. An open-collector or open-drain device is recommended to control this input.

Turn Q1 on applies a low voltage to the EN pin and disables the output of the supply, shown in figure 31. If Q1 is truns off, the supply executes a soft-start power up sequence, as shown in figure 32. A regulated output voltage is produced within 10ms.

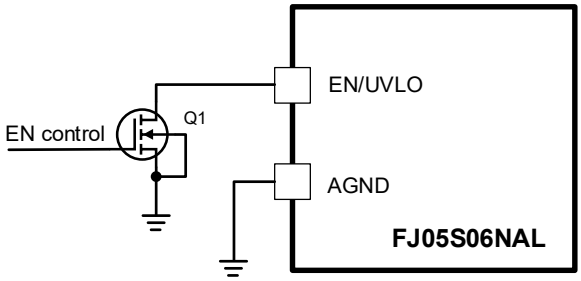


Figure 30. Typical Enable Control

Figure 43. 3.3Vin, 1.0Vout, 3A load, EN turn on	Figure 44. 3.3Vin, 1.0Vout, 3A load, EN turn off
Figure 45. 3.3Vin, 1.5Vout,3A load, EN turn on	Figure 46. 3.3Vin, 1.5Vout,3A load, EN turn off
Figure 47. 3.3Vin, 2.5Vout,3A load, EN turn on	Figure 48. 3.3Vin, 2.5Vout,3A load, EN turn off
Figure 49. 5.0Vin, 1.2Vout, 3A load, EN turn on	Figure 50. 5.0Vin, 1.2Vout, 3A load, EN turn off
Figure 51. 5.0Vin, 1.8Vout,3A load, EN turn on	Figure 52. 5.0Vin, 1.8Vout,3A load, EN turn off
Figure 53. 5.0Vin, 3.3Vout,3A load, EN turn on	Figure 54. 5.0Vin, 3.3Vout,3A load, EN turn off

8.10 Soft start

Leaving SS pin open enables the internal SS capacitor with a slow start interval of approximately 2ms. Adding additional capacitance between the SS and AGND increase the slow start time. Table 8. Shows an additional SS capacitor connected to AGND. See table 8. Below for SS values and time interval.

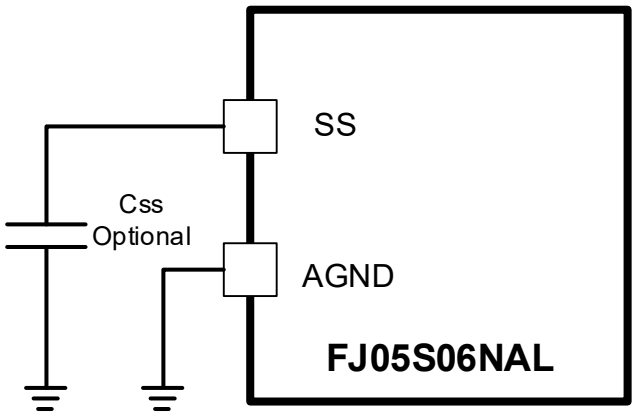


Figure 33. slow start capacitor (Css) connection

Table 9. slow-start capacitor values and slow-start time

Css (nF)	Open	2.2	4.7	10	15	22	47
SS time (ms)							

8.11 Overcurrent Protection

For protection against load faults, the FJ05S06NAL uses current limiting. The device is protected from overcurrent conditions by cycle-by-cycle current limiting. During an overcurrent condition the output current is limited and the output voltage is reduced, as shown in figure 33. When the overcurrent condition removed, the output voltage returns to the established voltage, as shown in figure 34.

3.3Vin, 1.0Vout, overcurrent limiting	3.3Vin, 1.0Vout, removal of overcurrent condition
3.3Vin, 1.5Vout, overcurrent limiting	3.3Vin, 1.5Vout, removal of overcurrent condition
3.3Vin, 2.5Vout, overcurrent limiting	3.3Vin, 2.5Vout, removal of overcurrent condition
5.0Vin, 1.2Vout, overcurrent limiting	5.0Vin, 1.2Vout, removal of overcurrent condition
5.0Vin, 1.8Vout, overcurrent limiting	5.0Vin, 1.8Vout, removal of overcurrent condition
5.0Vin, 3.3Vout, overcurrrent limiting	5.0Vin, 3.3Vout, removal of overcurrent condition

1.1 Sequencing

1.1.1 Figure1. sequencing schematic

1.1.2 Figure2. sequencing waveform

1.1.3 Figure3. Simultaneous tracking schematic

1.1.4 Figure4. Simultaneous tracking waveform

8.12 Programmable Undervoltage Lockout (UVLO)

The FJ05S06NAL implements internal UVLO circuitry on the VIN pin. The device disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO rising threshold is 4.5V (max) with a typical hysteresis of 150mV.

If an application requires either a higher UVLO threshold on the VIN pin, the UVLO pin can be configured as shown in figure 41.

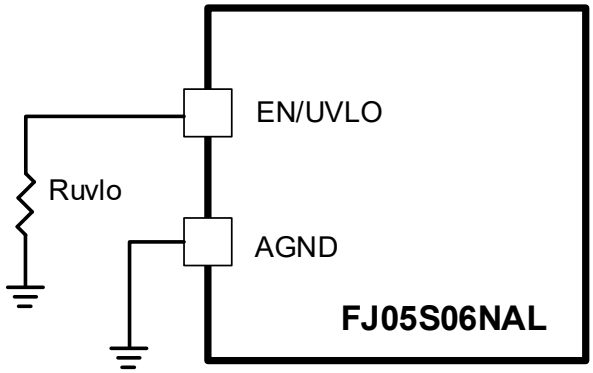


Figure 41. adjustable VIN UVLO

Table 10. standard resistor value for adjusting VIN UVLO

VIN UVLO (V)	2.8	3.0	3.2	3.6	4.0	4.5
Ruvlo (kΩ)						
Hysteresis (V)						

8.13 Thermal shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175℃ typically. The device reinitiates the power up sequence when the junction temperature drops below 165℃ typically.

8.14 Layout considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 44. Shows a typical PCB layout. Some considerations for an optimized layout are:

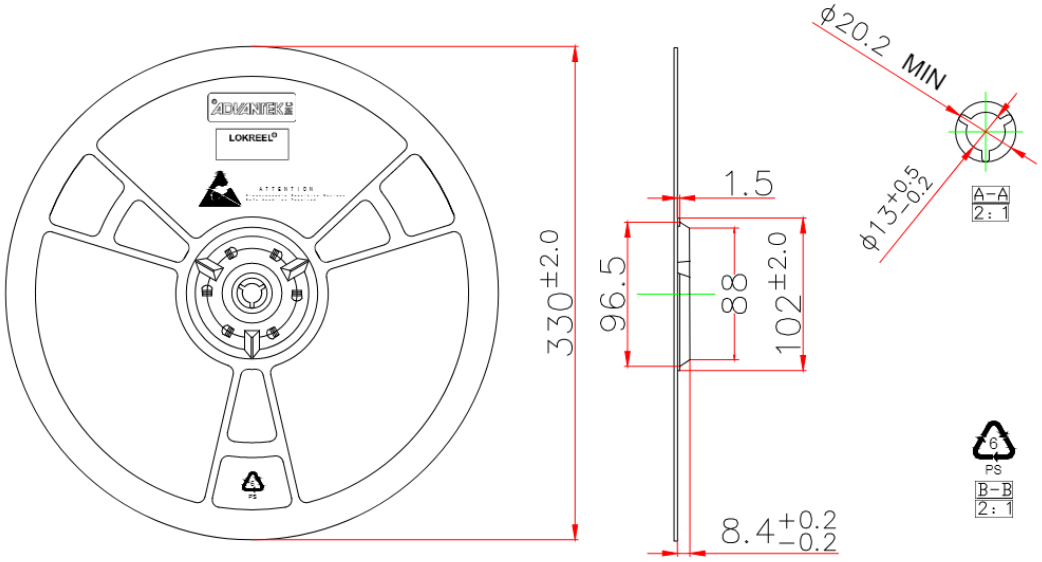
- Use large copper areas for power planes (VIN, VOUT, and GND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors closed to device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place a dedicated AGND copper area beneath the FJ05S06NAL.
- Isolate the SW copper area from the VOUT copper area at one point, near the output capacitor.
- Place Rset, Css as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

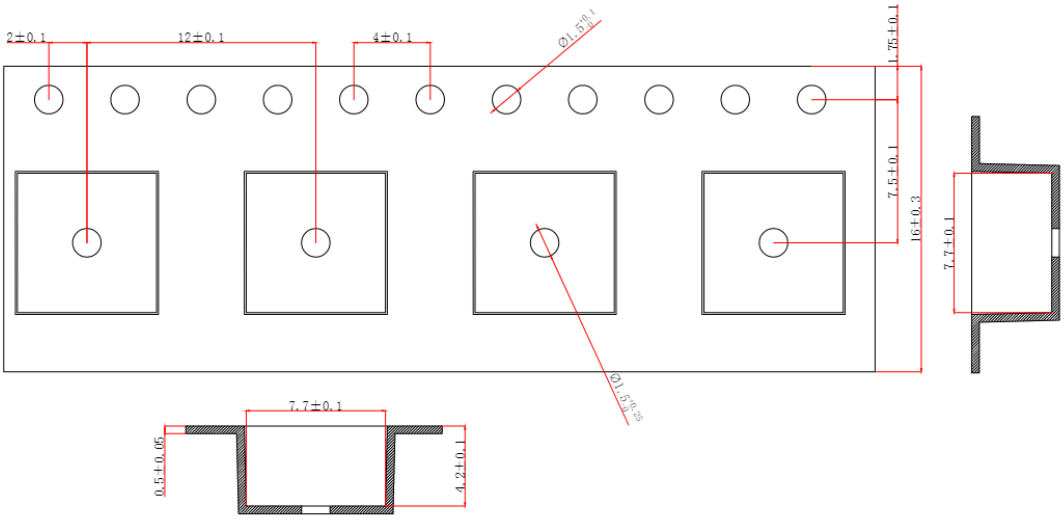
9 Revision History

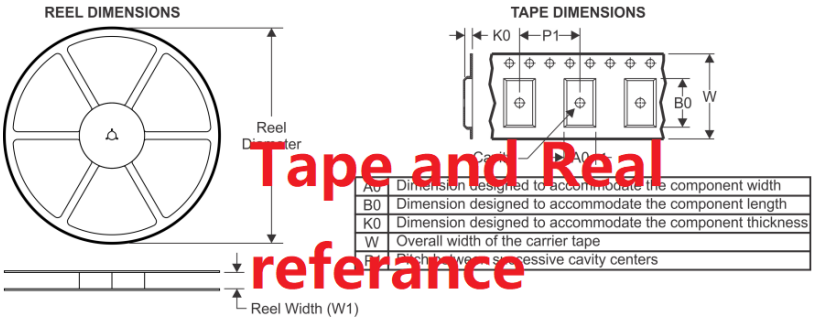
10 Documentation Support

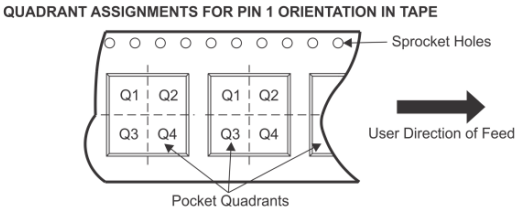
11 Mechanical, package, and Order information

12 Tape and Reel information









13 Package information